ARGUMENTS/REMARKS

STATUS OF CLAIMS

Claims 1 – 19 are pending.

Claims 1 – 2 are withdrawn from consideration.

Claims 3 and 5 – 19 stand rejected.

Claim 4 stands objected to.

No claims have been amended.

Prosecution History

This paper is filed in response to the **seventh** Office Action in this application. During prosecution, independent claims 3 and 10 have never been amended, and no RCE has been filed. Rather, the Office has repeatedly withdrawn its rejections and, instead of issuing a Notice of Allowance, issued a rejection on new grounds. The Office is respectfully requested to cease delaying this case, and promptly issue a Notice of Allowance.

Allowable Subject Matter

The indication that claim 4 would be allowable upon rewriting as an independent claim incorporating all of the limitations of base claim 3 is gratefully acknowledged.

Rejection of claims 3 and 5-19

Claims 3 and 5-19 stand rejected under 35 U.S.C. 103 as being unpatentable over U.S. Patent No. 6,787,826 (Tserng) in view of U.S. Patent No. 6,274,893 (Igarashi). The rejection is respectfully traversed, for at least the reason that the combination proposed by the Examiner would not result in an integrated circuit having all of the limitations of the rejected claims.

Claim 3 recites:

3. An integrated circuit, comprising:
   a. a first block comprising an enhancement mode pHEMT transistor on a substrate;
   b. a second block comprising a depletion mode pHEMT transistor on the substrate, the second block operatively connected to the first block; and
   c. a third block comprising a power pHEMT transistor on the substrate, the third block operatively connected to at least one of the first block and the second block.

As to claim 3, the Examiner states that Tserng discloses a first block comprising an enhancement mode PHEMT transistor on a substrate, and a second block comprising a depletion mode PHEMT transistor on the substrate. The Examiner concedes that Tserng fails to teach a power PHEMT transistor.

The Examiner's characterization of Tserng is simply wrong. Tserng does not disclose a pHEMT, i.e., a pseudomorphic HEMT, of any description, let alone an enhancement mode pHEMT and a depletion mode pHEMT. Rather, Tserng merely discloses a metamorphic HEMT (see col. 2, lines 45-47).

In addition to the failure of Tserng to disclose any pseudomorphic HEMT, Tserng fails to disclose a depletion mode HEMT and an enhancement mode HEMT on the same substrate. Rather, Tserng explicitly calls for different substrates to support these different types of HEMTs. Tserng states, at col. 5, lines 27-31: "If Schottky layer 14 is thin (e.g., less than about 100 Å), HEMT 2 operates as an enhancement mode transistor. If Schottky layer 14 is made thicker (e.g., more than about 100 Å), HEMT 2 operates as a depletion mode transistor." Thus, in Tserng, different substrates, with different thicknesses of Schottky layer, are required to obtain even two different HEMTs.

The foregoing represents sufficient grounds for withdrawal of the rejection of claim 3 and allowance of that claim. For completeness, Applicant will point out additional grounds for withdrawal of the rejection.

The Examiner states that Kim discloses a high electron mobility transistor with a third block comprising a power PHEMT transistor on the substrate, the third block operatively connected to at least one of the first block and the second block. Applicant understands that the Examiner intended to cite Igarashi, and not Kim. The Examiner states that it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of Tserng and Kim (again, Applicant understand that the Examiner intended to cite Igarashi and not Kim) to form a transistor since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. The Examiner states that doing so would facilitate the manufacture of the semiconductor device and enhance the performance of the semiconductor transistor.

The Examiner's characterization of Igarashi is also incorrect. Igarashi does not disclose a pseudomorphic HEMT of any description. Rather, Igarashi discloses HEMTs (see Abstract). For this additional independent reason, the rejection of claim 3 should be withdrawn, and claim 3 should be allowed.

Furthermore, Tserng and Igarashi disclose different substrates, such that the combination thereof could not result in transistors of *any* type on the same substrate.

The Office Action proposes combining Tserng with the structure shown in Igarashi at Figs. 14H-14K. As the respective substrates are different, the proposed combination is not possible. For example, the substrate of Tserng has a substrate 4;

buffer layer 6 on substrate 4; heavily doped p-type barrier layer 8 on buffer layer 6; spacer layer 10, of undoped InAlAs (col. 4, lines 35-36) on barrier layer 8; channel layer 12, either having three composite sublayers or of uniform composition, of InGaAs (col. 4, lines 48-67) on spacer layer 10; Schottky layer 14 of n-type doped InAlAs (col. 5, lines 15-20) on channel layer 12; and cap layer of heavily doped n-type InGaAs (col. 5, lines 39-41), which may be patterned to provide source and drain contacts (see col. 2, line 62, to col. 3, line 5). In contrast, the substrate of Fig. 14K of Igarashi has a buffer layer of undoped AlGaAs beneath its channel layer (col. 16, lines 59-67), in contrast to the spacer layer of undoped InAlAs of Tserng. Igarashi has an electron supply layer 55 of n+ AlGaAs on its channel layer (col. 16, lines 63-65), and a Schottky layer 56 of n-AlGaAs on the electron supply layer; in contrast, Tserng has a Schottky layer of InAlAs directly on its channel layer. Igarashi has an n+ GaAs cap layer, while Tserng has a cap layer of InGaAs.

In short, the proposed combination is not possible, as Tserng and Kim teach two different substrates. For this additional reason, the rejection of claim 3 should be withdrawn, and claim 3 should be allowed.

Furthermore, the proposed rationale for obviousness is not appropriate. The Examiner proposes to form a transistor. However, Tserng and Igarashi each separately already teaches a transistor; accordingly, there is no need to combine Tserng and Igarashi to form a transistor. Furthermore, there is no duplication of components between Tserng and Igarashi, as the two references teach differing and non-duplicative substrates. Still further, there is no explanation provided as to how a proposed combination of Tserng would facilitate the manufacture of the

semiconductor device or enhance the performance of a semiconductor transistor. Indeed, since it is not possible to combine the differing substrates of Tserng and Igarashi, the proposed combination would not serve these purposes.

In short, for at least the independently sufficient reasons that: (1) the rejection mischaracterizes Tserng; (2) the rejection mischaracterizes Igarashi; (3) the proposed combination of Tserng and Igarashi is impossible, and (4) there is no proper rationale for a finding of obviousness, the Examiner has failed to provide a proper *prima facie* case of obviousness as to claim 3.

For at least the foregoing reasons, claim 3 is allowable over the prior art of record.

Claim 5-6 depend from claim 3, and are allowable at least by virtue of their dependence from an allowable base claim.

Claim 7 is an independent claim reciting an analog to digital converter, having an enhancement mode pHEMT device, a depletion mode pHEMT device, and a power pHEMT device on a single substrate. For the reasons discussed above in connection with claim 3, the Examiner has not provided a proper *prima facie* case of obviousness as to a circuit having these three types of devices formed on a single substrate. For at least this reason, claim 7 is allowable.

Claims 8 and 9 depend from claim 7, and are allowable at least by virtue of their dependence from an allowable base claim.

Claim 10 is an independent claim that includes all of the limitations of claim 3, and is allowable at least for the reasons that claim 3 is allowable.

Claims 11 – 15 and 17 - 19 depend directly or indirectly from claim 3, and are allowable over the prior art of record at least by virtue of their dependence from an allowable base claim.

Claim 16 depends indirectly from claim 3, and further recites that the recess of the power pHEMT transistor is a double recess, that the recess of the depletion mode pHEMT transistor is a single recess, and that each of the recesses is defined through at least one common layer of the substrate. There is no teaching or suggestion in either Tserng or Igarashi of a power pHEMT transistor having a double recess and a depletion mode pHEMT transistor having a single recess, each of those recesses defined through at least one common layer of a substrate. For at least these reasons, as well as by virtue of its dependence from allowable base claim 3, claim 16 is allowable.

CONCLUSION

Wherefore, Applicant believes he has addressed all outstanding matters, and respectfully requests that claims 3 – 19 be allowed.

Should there be any questions or outstanding matters, the Examiner is cordially invited and requested to contact Applicant's undersigned attorney at his number listed below.

Respectfully submitted,

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